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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,190	03/18/2004	Shunpei Yamazaki	0756-7269	5109

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EXAMINER	
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ART UNIT	PAPER NUMBER
2629	

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11/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,190	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	MY-CHAU T. TRAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *2-5,8,9,12,13 and 15-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,10,11,14 and 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application and Claims Status

1. Applicant's response filed 08/10/2009 are acknowledged and entered.

2. Claims 1-31 were pending. Applicants have added claims 32-37. No claims were amended and/or cancelled. Therefore, claims 1-37 are currently pending. Claims 2-5, 8, 9, 12, 13, and 15-22 are drawn to non-elected species and/or inventions, wherein the election was made *with* traverse in the reply filed on 05/16/2007, and thus these claims remain withdrawn from further consideration by the examiner, 37 CFR 1.142(b), there being no allowable generic claim. Accordingly, claims 1, 6, 7, 10, 11, 14, and 23-31 are under consideration in this Office Action.

Maintained Rejection(s)

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 6, 7, 10, 11, 14, and 23-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishitoba et al. (US Patent 6,774,877) in view of Yamazaki (US Patent Application Publication US 2002/0047825 A1).

For ***claims 1, 6, 7, 10, 11, 14, and 23-31***, Nishitoba et al. disclose an organic electroluminescent (EL) image display device (see e.g. Abstract; col. 1, lines 7-12; col. 3, line 49 thru col. 4, line 14; fig. 3). As illustrated by figure 3, the device comprises an organic EL element (ref. #11) (refers to instant claimed light emitting element/pixel electrode) and two

transistors (ref. #8 and 9) (refers to instant claimed first and second transistors) connected to the organic EL element in a series (see e.g. col. 6, lines 17-59). The anode of the organic EL element (ref. #11) is connected to the drain (refers to instant claimed limitation of '*one of a source region and a drain region of the first transistor is connected to the light emitting element*') of transistor (ref. #8)(refers to instant claimed first transistor) and the source of transistor (ref. #8) is connected to the drain of transistor (ref. #9)(refers to instant claimed second transistor) (refers to instant claimed limitation of '*the other one of the source region and the drain of the first transistor is connected to one of a source re(lion and a drain region of the second transistor*') (see e.g. col. 6, lines 17-27; fig. 3). Additionally as illustrated by figure 3, the device comprise a switching transistor (ref. #12) (refers to instant claimed third transistor) wherein the drain (refers to instant claimed first electrode of the third transistor) is connected to the signal line (ref. #3) and the source (refers to instant claimed second electrode of the third transistor) is connected to the gate electrodes of both transistors (ref. #8 and 9) (see e.g. col. 6, lines 28-36). The gates of the transistors (ref. #8 and 9) are connected to each others (refers to instant claimed gate electrodes) and they are p-channel MOS transistors (refers to instant claimed p-type transistor/same polarity) (see e.g. col. 6, lines 24-25 and 39-40; fig. 3). Nishitoba et al. disclose that the transistor (ref. #9) compensates the variations in the threshold voltage of the transistor (ref. #8) (see e.g. col. 6, lines 38-59). The transistor (ref. #8) operates in the saturation region, and the transistor (ref. #9) operates in the non-saturation region, i.e. linear region (see e.g. col. 6, lines 38-59). Nishitoba et al. also disclose that the channel width of transistors of references #6 to #9 is 4 μm, i.e. constant (see e.g. col. 7, lines 42-44). As shown in figure 6, there is a relationship between the channel length of transistors of references #7 and #9 and the

variations in output current such that the desired characteristics can be obtained by selecting the channel length of transistors of references #7 and #9 according to the picture quality that is demanded of the image display device (see e.g. col. 6, lines 38-59; col. 7, lines 23-57), which imply that the size of the transistor's channel, i.e. length and width, would be a choice of experimental design and is considered within the purview of the cited prior art. Moreover, Nishitoba et al. disclose that the channel length of transistors of references #7 and #9 can be set to at least 0.5 times or at least one time but not greater than four times the channel length of transistors of references #6 and #8, i.e. if the channel length of transistor (ref. #9) is set at 15 μm then the channel length of transistor (ref. #8) is 7.5 μm such that the channel length of transistor (ref. #9) is 0.5 times that of the channel length of transistor (ref. #8) (see e.g. col. 7, lines 54-57).

For ***claims 11, and 25***, Nishitoba et al. disclose the method of driving the light emitting device wherein the step comprises controlling the current to be supplied to a light emitting device by the first and second transistors (see e.g. col. 3, line 49 thru col. 4, line 14; col. 6, line 60 thru col. 7, line 22; figs. 3 and 4). Moreover, Nishitoba et al. disclose the claimed structural features of the instant claimed light emitting device as discussed above.

The teachings of Nishitoba et al. differ from the presently claimed invention as follows:

For ***claims 1, 7, 11, and 23-25***, Nishitoba et al. fail to disclose the limitation that '*wherein the first transistor and the second transistor share a same semiconductor island*', i.e. the first and second transistors are formed on the same semiconductor layer/island.

However, Yamazaki teach the limitations that are deficient in Nishitoba et al. as follows:

For ***claims 1, 7, 11, and 23-25***, Yamazaki discloses a method for manufacturing semiconductor device with thin film transistor (TFT) (see e.g. Abstract; sections: [0002] and

[0017]-[0022]; figs. 1A-1D and 2A-2E). The method produces two TFT on a substrate (see e.g. sections: [0043] thru [0066]; fig. 2E). The method comprises the steps of forming a silicon oxide film (refers to instant claimed semiconductor island) on a substrate and forming gate electrodes (ref. #103 and 104) on the silicon oxide film (see e.g. sections: [0043]-[0044]; fig. 1A). Furthermore, Yamazaki defines the term of semiconductor device to include electro-optical devices wherein these electro-optical devices include display devices such as electroluminescence (EL) display device (see e.g. sections: [0003], [0257], and [00258]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to disclose that the first and second transistors are formed on the same semiconductor island as taught by Yamazaki in the device of Nishitoba et al. One of ordinary skill in the art would have been motivated to the first and second transistors are formed on the same semiconductor island in the device of Nishitoba et al. for the advantage of providing semiconductor device that include bottom-gate TFTs (Yamazaki: section [0014]). Additionally, both Nishitoba et al. and Yamazaki disclose display device with p-channel thin film transistor (TFT) (Nishitoba: col. 5, line 62 thru col. 6, line 16; Yamazaki: sections: [0003], [0257], and [00258]). Furthermore, one of ordinary skill in the art would have a reasonable expectation of success in the combination of Nishitoba et al. and Yamazaki because forming two transistors onto the same island is known in the art, if for no other reason to make the manufacturing process simpler.

Therefore, the combine teachings of Nishitoba et al. and Yamazaki do render the device of the instant claims *prima facie* obvious.

Response to Arguments

5. Applicant's arguments directed to the above 103(a) rejection were considered but they are not persuasive for the following reasons.

[1] Applicant contends that the references of Nishitoba et al. and Yamazaki, "*either alone or in combination, does not teach or suggest all the features of the independent claims 1, 7, 11 and 23-25*" that "*recite a same semiconductor island*" for "*A silicon oxide film is not a semiconductor island. Yamazaki '825 merely discloses "a silicon oxide film 102 as an underlayer film 102" (¶ [0044])*".

Thus, the combine references of Nishitoba et al. and Yamazaki is *prima facie* obvious over the instant claimed inventions.

This is not found persuasive for the following reasons:

[1] The examiner respectfully disagrees. It is the examiner's position that the combine teachings of Nishitoba et al. and Yamazaki do render the invention of the instant claims *prima facie* obvious. First, the limitation of '*the first transistor and the second transistor share a same semiconductor island*' of independent claims 1, 7, 11, and 23-25 would encompass the interpretation that the "*semiconductor island*" is an additional layer on top of a substrate on which "*the first transistor and the second transistor*" are formed. Here, Yamazaki disclose a silicon oxide film (ref. #102) is formed on a substrate and gate electrodes (ref. #103 and 104) of the transistors on the silicon oxide film, and as a result, the reference of Yamazaki does disclose the limitation of '*the first transistor and the second transistor share a same semiconductor island*' of independent claims 1, 7, 11, and 23-25. Moreover, the instant claimed specification does not specifically define the term "*semiconductor island*" such that it would exclude this

interpretation. Second, applicant's arguments do not rise to the level of factual evidence. See MPEP § 716.01(c): The arguments of counsel cannot take the place of evidence in the record. *In re Schulze*, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965). That is applicant's arguments are conclusionary, i.e. applicant has not explained how the silicon oxide film of Yamazaki is ***not*** a "*semiconductor island*", and applicant did not explain what the improvement is over the prior art of record.

Therefore, the combine teachings of Nishitoba et al. and Yamazaki do render the invention of the instant claims *prima facie* obvious, and the rejection is maintained.

New Rejection(s) – Necessitated by Amendment

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 32-37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s) at the time the application was filed had possession of the claimed invention. (This is a new matter rejection.)

Claims 32 and 37 recite the limitation of '*the semiconductor island comprises a channel forming region of the first transistor and the second transistor*'. This limitation, which narrows the structural feature of the instant claimed "*semiconductor island*", is not supported by the

originally filed specification and/or claims; nor has applicant provided any indication where such support exists. See MPEP § 714.02, 5th paragraph, last sentence; MPEP § 2163.02; and MPEP § 2163.06. For example, the originally filed specification discloses that '*The driving transistor which is shown in Fig. 6 includes an active layer 601, a gate insulating layer 602 which is in contact with the active layer 601, and a gate electrode 603 which is overlapped with the active layer 601 with the gate insulating layer 602 therebetween*' and '*The active layer 601 includes a channel forming region 604 which is overlapped with the gate electrode 603 with the gate insulating layer 602 therebetween*' (see original specification paragraph [0050]-[0051]). Therefore, the originally filed specification does not provide support for this limitation. Furthermore, the original claims do not recite this limitation, i.e. '*the semiconductor island comprises a channel forming region of the first transistor and the second transistor*'. Consequently, this limitation has no specification or original claim support, and it is considered new matter.

If applicants disagree, applicant should present a detailed analysis as to why the claimed subject matter has clear support in the specification.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MY-CHAU T. TRAN whose telephone number is 571-272-0810. The examiner can normally be reached on Monday: 8:00-2:30; Tuesday-Thursday: 7:30-5:00; Friday: 8:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MY-CHAU T. TRAN/
Primary Examiner, Art Unit 2629

November 13, 2009